REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-15 are now in the application. Claim 1 has been amended. Claim 15 has been added.

In item 3 on pages 2-4 of the above-mentioned Office action, claims 1-7 have been rejected as being unpatentable over Hirota et al. (US 6,316,329 B1) in view of Nishioka et al. (US 5,489,548) or Vaartstra (US 6,225,237 B1) under 35 U.S.C. § 103(a).

In item 4 on pages 4-5 of the above-mentioned Office action, claims 1-7 have been rejected as being unpatentable over Clevenger et al. (US 6,348,395 B1) in view of Nishioka et al. or Vaartstra under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references. However, the language claim 1 has been modified in an effort to even more clearly define the invention of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> providing a configuration including a semiconductor substrate, a first layer configuration configured on the semiconductor substrate, a second layer configured on the first layer configuration, and a third layer configured on the second layer, the first layer configuration being a ferroelectric or dielectric layer configuration of a plurality of individual layers including an upper layer having a metal, a middle layer having barium-strontium-titanate, and a lower layer having iridium or iridium oxide;
>
> patterning the third layer to form a first trench, which uncovers the second layer, in the third layer;
>
> using the third layer as an etching mask, etching the second layer and forming a second trench in the second layer near the first trench, the second trench uncovering the upper layer of the first layer configuration;
>
> removing the third layer from the second layer;
>
> using the second layer as an etching mask, etching all of the plurality of individual layers of the first layer configuration and forming a third trench in all of the plurality of individual layers of the first layer configuration, the third trench being formed near the second trench and uncovering the substrate;
>
> after forming the third trench, depositing a fourth layer of an insulating material on the semiconductor substrate;
>
> chemically-mechanically polishing the fourth layer and then the second layer to remove the fourth layer from the second layer and then to remove the second layer from the upper layer of the first layer configuration, the fourth layer remaining in place in the third trench.

According to claim 1, the invention of the instant application relates to a process in which a layer stack including layers

(21, 22, 23) is to be etched with respect to a hard mask layer (3). The layer stack (21, 22, 23) includes an upper layer including metal, a middle layer including barium-strontium-titanate or strontium-bismuth-tantalate, and a lower layer including iridium or iridium oxide. Having etched the layer stack (21, 22, 23), the corresponding trench is filled with a fourth layer (8) of an insulating material. Then, the fourth layer is removed and the second layer is removed (which is the hard mask). This results in a structure as shown in Fig. 6, where the layer (2) of Fig. 6 is actually a layer stack including layers similar to the layers (21, 22, 23) of Fig. 7.

Applicants believe that the Examiner has taken a very formalistic approach when he attempts to combine the teachings of Hirota et al. and Nishioka et al. or Vaartstra, or in the alternative attempts to combine Clevenger et al. and Nishioka et al or Vaartstra. Applicants believe that Hirota et al. and Clevenger et al., on one hand, and Nishioka et al. and Vaartstra, on the other hand, relate to different processes and there is no link between them which would encourage a person skilled in the art to transfer the technical teaching from Nishioka et al. or Vaartstra to Hirota et al. or Clevenger et al., for the reasons that are discussed below.

Hirota et al. describe the formation of shallow trench isolation (see Figs. 3C - 3G). The layer stack 102, 103, 104 to be etched includes silicon oxide 102, diamond-like carbon 103, and amorphous silicon 104 (see column 6, first paragraph).

Nishioka et al. in fact describe a ferroelectric layer stack including layers 42, 44, 46, for example made of iridium, barium-strontium-titanate, platinum (see the table in column 9). It becomes apparent from Fig. 12 that the only layer to be patterned is the lower layer 42. The middle and the upper layers 44 and 46, respectively, are continuous layers practically covering the full wafer, a portion of which is shown in Fig. 12. At least, Fig. 12 does not show that layers 44 and 46 would have to be patterned. Thus, a person skilled in the art would not be encouraged to use the layer stack 42, 44, 46 of Nishioka et al. in the environment of Hirota et al. As is clearly shown in Hirota et al., all three layers 102, 103, 104 are patterned and removed within the trench 110 to be etched, while layers 44 and 46 of Nishioka et al. must not be etched.

A layer stack including metal, barium-strontium-titanate or strontium-bismuth-tantalate and another layer of iridium or iridium oxide is known to a person skilled in the art.

Nothing else is disclosed in Nishioka et al. However, the invention of the instant application claims the etching of all three layers 21, 22, 23, the coverage with a fourth layer of isolation material, and the subsequent processing by CMP. Nishioka et al. provide no hint to use the layer stack 42, 44, 46 in the shallow trench isolation structure of Hirota et al.

Vaartstra describes a ferroelectric capacitor (Fig. 1) where the capacitor layer stack of layers 13, 11, 12 is patterned. However, while the invention of the instant application claims a CMP process wherein the fourth layer and the hard mask etching layer are chemically-mechanically polished, such a process step cannot be determined in connection with Fig. 1 of Vaartstra since the isolating layer (no reference symbol available), which covers layer stack 13, 11, 12, covers layer 12 and extends beyond layer 12 so that it is not planarized with layer 12. Planarization, however, is the case in Fig. 3G of Hirota et al. as well as in Fig. 6 of the invention of the instant application. Applicants, therefore, believe that a person skilled in the art would not be encouraged to use the teaching of Vaartstra in the environment of Hirota et al.

Clevenger et al. disclose a process (Figs. 3A to 3D) similar to the process disclosed in Hirota et al. For example, the

layer 260 may be silicon-germanium, the layer 270 may be an oxide layer, and the layer 220 may be diamond-like material. All of this is not the claimed layer stack of the invention of the instant application, which includes metal, barium-strontium-titanate or strontium-bismuth-tantalate and iridium or iridium oxide according to claim 1 of the instant application. Hence, the arguments as set forth above relating to Hirota et al., Nishioka et al. and Vaartstra apply to the rejection in item 4 of the Office Action in a similar way.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since claims 2-7 are dependent on claim 1, they are believed to be patentable as well.

Claim 15 has been added. Since none of the references discloses strontium-bismuth-tantalate, claim 15 is believed to be patentable.

In view of the foregoing, reconsideration and allowance of claims 1-7 and 15 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

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August 24, 2005

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